

10/098551



PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10098551	FILING DATE 03/18/2002	CLASS 716	SUBCLASS 6	GAU 2825	EXAMINER DC
**APPLICANTS: Matsumoto Sho;					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED: JAPAN 2001-291413 09/25/2001 YES					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO	
Verified and Acknowledged Examiners's initials TD		1450.1019			
TITLE : Design system of integrated circuit and its design method and program					

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		THUAN DO Assistant Examiner	CLAIMS ALLOWED	
			Total Claims 20	Print Claim for O.G. 1
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drwg. 6	Figs. Drwg. 9
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
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